

**SanDisk Corporation**

**Systems Engineering Department**

**C O N F I D E N T I A L**

**32nm X3 support for SD/MS based on PhoenixC2Up9**

**Requirements Document**

**EPRD**

()

|  |  |  |  |
| --- | --- | --- | --- |
| **REVISION HISTORY** | | | |
| **Rev.** | **Author** | **Reason for Change** | **Date** |
| 0.1 | David Zehavi | Initial Draft Version | Nov-27-08 |
| 0.2 | David Zehavi | * Change risks table * Update PhoenixC2 Schedules * Add 52b ECC for 32nm D2 * Add USB support on PhoenixC2 * Support of SD 3.0 | Jan-11-09 |
| 0.3 | Georgi Todorov  Orna Petruschka | * Update approval list * ACT date to Dec/30 * Add MS High-Performance Requirements * MS-HG ROI justification * Removal of HSI * Add SD Lightening * Add MMC speed class * Update # flash dies supported * Power section update * Change to product priority * Open issues section |  |
| 0.4 | Orna Petruschka | * Update resource section * Update approval list * Change ACT date * ASIC to support 50MB/sec throughput * ASIC process removed (not part of EPRD requirement) * Memory footprint update * Changed supported flash list * Add controller power * Updated iNAND inputs from marketing – performance, speed class, endurance, ESD | Mar-5-09 |
| 0.5 | Orna Petruschka, David Zehavi | * Updated RAM sizes, schedules, product performance, controller power, SD priorities * Added ASIC support for 24nm X3 * Adding packaging resources, UHS-104 , AFM Support | Aug-31-09 |
| 0.6 | Nadav Grosz | * Updated SW dev. Cost * Added Lightning support * Added MMC and SD with X3 performance * UHS-104 support limitation and constraints | 12-Nov-09 |

**Approvals:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Title** | **Name** | **Signature** | **Date** |
| EVP, GM OEM Business & Corporate Engineering | Yoram Cedar |  |  |
| VP, Corporate Engineering | Simon Stolero |  |  |
| VP, Packaging and Assembly | Hem Takiar |  |  |
| VP, Product Test | Larry Rowland |  |  |
| Quality and Reliability | Arun Malhotra |  |  |
| Sr. Dir, ASIC Development | Stan Chapski |  |  |
| Sr. Dir, Firmware Development | Carlos Gonzalez |  |  |
| Dir, SDMMC R&D Manager | Reuven Elhamias |  |  |
| BE System | Jian Chen |  |  |
| SVP, Memory Technology & Memory Product Development | Khandker Quader |  |  |
| Memory device/process/ technology Development | Khandker Quader |  |  |
| PLM, MS | Mike McCarthy |  |  |
| PLM, SD | Yosi Zatelman |  |  |
| SVP, Finance | Milo Azarmsa |  |  |
| Corporate PM, | Mike Morganstern |  |  |
| Marketing, MIV | Oded Sagee |  |  |

**Table Of Contents**

[Section I. Executive Summary 5](#_Toc245789411)

[Section II. Strategy 6](#_Toc245789412)

[Section III. Technology Profile 7](#_Toc245789413)

[Section IV. Risks 11](#_Toc245789414)

[Section V. Development Cost 12](#_Toc245789415)

[Section VI. Appendix – Major Decisions 13](#_Toc245789416)

[Section VII. Appendix – Open Issues 14](#_Toc245789417)

[Appendix A MMC random performance 15](#_Toc245789418)

[Appendix B ESD Requirements 16](#_Toc245789419)

[Appendix C Memory Configurations 17](#_Toc245789420)

[Appendix D UHS-104 support limitations and constraints 19](#_Toc245789421)

# Section I. Executive Summary

The following EPRD sets the requirements for the PhoenixC2Up9 controller.

PhoenixC2Up9 is designed to be a low cost SD and MS controller targeted specifically for SD blue label (3.0/5.0MB/sec) and M2 Mobile Standard (3.0/6.0MB/sec) card performance with 32nm X3/EX3 and 24nm X2 memory.

PhoenixC2Up9 is designed also to support M2 Mobile Ultra (6/18MB/sec), SD Ultra (7/15MB/sec), SD Lightening (30/30MB/sec), MS High-Performance (a combined SKU for ProHG 30MB/s and VideoHD/Mark2 15MB/s), iNAND eMMC4.4 boot & storage (up to 9/30MB/sec) and SD UHS-50 performance (30/30 MB/Sec).

This controller is designed to compete with SanDisk low cost controller competitors.

PhoenixC2Up9 die cost target is <$0.13

PhoenixC2Up9 ASIC architectures will be based on PhoenixC1Up9 and Gen6 FW architecture optimized to support a low cost controller with SanDisk’s memory support of 32nm X1/X2/X3/EX3, 24nm X1/X2, ASIC/ROM support for 24nm X3 (if 122-bit ECC is sufficient) and Samsung memory.

The ASIC will support MS and SD as follows:

**Memory Stick**

PhoenixC2Up9 will support legacy MS PRO Duo, MS Pro-HG and Memory Stick Micro (M2). Specifics are presented later in this document.

**SD**

PhoenixC2Up9 will support SD/SDHC/SDXC, microSD and MMC. Specifics are presented later in this document.

**eMMC**

PhoenixC2Up9 will support legacy iNAND eMMC4.3 features as well as the eMMC4.4 spec. Specifics are presented later in this document

Target tape-out date is Aug 31, 2009.

# Section II. Strategy

|  |  |
| --- | --- |
| Goals | 1. Develop controller to support 32nm X3/EX3 and 24nm X 2 memories. 2. Develop low cost controller for Ultra performance for SD, eMMC and MS. 3. Develop controller that will support SD 3.0 up to UHS-I performance 4. Develop controller to support eMMC 4.4 Specification 5. Develop a controller to support MS High-Performance (a combined SKU for ProHG, VideoHD and Mark2 channels) |
| Objectives | * Support new memory technology 32nm X3/EX3 and 24nm X2 * Support markets mainstream for 2010/2011 with the following products:   - SD/uSD blue label , Ultra, Extreme, Lightening, UHS-50 and UHS 104  - iNAND eMMC 4.4 for the OEM embedded markets (covering boot + storage)  - M2 Standard and Ultra  - eMS/eM2 for OEM embedded markets  - MS High-Performance for Ultra, Video and high-end Digital Imaging markets |
| Markets Addressed | 1. MS Duo, MS ProHG, eMS/eM2, MS M2, MicroSD, SD/SDHC/SDXC/eSD/eMMC |
| Development Strategy | * Controller ASIC architecture, firmware architecture to be developed by SanDisk Engineering. |
| Product Families | 1. Blue Line (3.0/5.0MB/sec) retail and generic OEM cards 2. Blue Line (5/15MB/sec) uSD custom OEM 3. Ultra/Mobile Ultra Line (7/15MB/sec) retail and generic OEM cards 4. Extreme (20/20MB/sec) 5. Lightning Line (30/30MB/sec) retail 6. SD UHS-50 (30/30MB/Sec) retail and generic OEM cards 7. iNAND eMMC boot & storage (up to 9.0/30MB/s) OEM Embedded 8. M2 Mobile Standard (3.0/6.0MB/sec) retail and generic OEM cards 9. M2 Mobile Ultra (6.0/18MB/sec) retail and generic OEM cards 10. MS High-Performance (15MB/s Ultra/VideoHD/Mark2 and 30MB/s ProHG) |
| Schedule Milestones | Tape-out Aug 31, 2009  Wafer Out Oct 15, 2009  Tested Parts Oct 22, 2009 Final FW ready Feb 25, 2010  ACT date Mar 30, 2010 |
|  |  |
|  |  |

# Section III. Technology Profile

|  |  |  |
| --- | --- | --- |
| Host IF | 1. SD 3.0 (SD, SDHC and SDXC(SD 2.0 and SD 1.1 - supported) 2. SD UHS-50: SDR50/DDR50 (SD 3.0) 3. SD UHS-104 4. MMC 4.4 and below (Including DDR52 IF) 5. MS Pro-Duo 6. MS ProHG 7. M2 | Please refer to appemdix D for UHS-104 limitation and constraints |
| Flash IF | 1. x8/x16 support | No HSI |
| MS Bus Speed | 1. MS Pro (x1) 20Mhz 2. MS Pro (x4) 40Mhz 3. MS ProHG (x8) 60Mhz |  |
| SDMMC Bus Speed | 1. SD Normal Speed 0 - 25Mhz 2. SD High Speed 0 - 50Mhz 3. SD Lightning 0-75Mhz 4. UHS50 modes (1.8V signaling)   SDR12  SDR 25  SDR 50  DDR 50  UHS 104 mode 0 – 208MHz   1. MMC Normal Speed 0 - 20Mhz; 0 – 26Mhz 2. MMC High Speed 0 - 52Mhz 3. MMC DDR52 0 - 52Mhz |  |
| SD, MMC,MS Performance Targets | 1. SD BL: uSD, SD: 5/5 MB/sec(X2), 3/5MB/sec (X3) 2. SD Ultra Low Speed: uSD, SD: 7/10 MB/sec (X2), 5/7 MB/sec (X3)SD Ultra High Speed: uSD, SD: 7/15 MB/sec (X2), 5/15 MB/sec (X3) 3. SD Extreme: 20/20 MB/s (X2) 4. SD UHS-50: uSD, SD: 30/30 MB/sec (X1,X2) 5. SD UHS-104: uSD, SD: 40/40 MB/sec(X1,X2) 6. SD Lightning: 30/30 MB/sec (X1, X2) 7. MMC normal mode: (0-26Mhz), power class0, 9MB/s write and 15MB/s read 8. MMC normal mode on X3 memory: (0-26Mhz), power class0, 5MB/s write and 15MB/s read 9. MMC high speed mode: (52Mhz), power class0, 9MB/s write and 30MB/s read 10. MMC special “side loading” mode: (52MHz; not exceeding power class 4) 20MB/s write and 40MB/s read. 11. MMC special “side loading” mode on X3 memory: (52MHz; not exceeding power class 4) 10MB/s write and 20MB/s read. 12. MMC random performance (52Mhz): On X2 memory: write: 150 accesses per second, read: 1000 accesses per second On X3/eX3 memory: write: 50 accesses per second, read: 1000 accesses per second 13. M2 BL: 3/6MB/sec 14. M2 MobileUltra: 6/18MB/sec 15. MS Duo BL: 5/10MB/s 16. MS Duo Mark2/VideoHD, eMS/eM2: 15/15MB/s (4MB/s worst case) 17. MS ProHG: 30/30MB/s (15MB/s worst case) | 1. ASIC to support 50MB/sec throughput for ECC up to 122-bit and ~100 bits errors. Otherwise, 37MB/sec. 2. See Appendix A for details on random performance |
| SD Speed Class /  MS Mark | 1. SD BL: Speed class 2 for capacities >=4GB 2. SD Ultra: Speed class 2/4/6 for capacities >=4GB 3. SD Lightning: Speed class 10 for capacities >=4GB 4. SD UHS-50: Speed class 10 for capacities >=4GB 5. MMC Speed Class C 6. MS Duo/M2 class 2 (1.875/1.875 MB/sec min) 7. MS Mark2 (4/4 MB/sec min) 8. MS ProHG x4 (5/5 MB/s min) 9. MS ProHG x8 (15/15 MB/sec min) | eMS/eM2 have Mark2 requirements but with a higher average power. |
| Capacities | 1. MS 2GB – 64GB 2. SD 2GB – 128GB 3. MMC 2GB – 64GB | 64GB – first products with exFAT |
| Primary Memory Used | 1. SNDK 32nm X1/X2/X3/EX3, x16, x8 2. SNDK 24nm X1/X2, x16, x8 3. SNDK 24nm X3 – ASIC support including ROM (to be ready if 122-bit ECC is sufficient) (FW support in future upon demand) 4. SNDK 43nm X1/X2, x16, x8 - ASIC support only including ROM (FW support in future upon demand) 5. Samsung 42nm 16G D2 single/dual die – ASIC support only including ROM (FW support in future upon demand) 6. Samsung 3xnm X2/X3 – ASIC support, including ROM, for all available datasheets up to date (those that toggle mode is not mandatory) | * Support backup ID scheme for memories not available in the ROM table * See Appendix C for a full list |
| Flash dies # / Flash configurations | 1. Maximum of 16 flash dies 2. Die interleave as needed with power consumption limitation 3. Plane interleave as needed 4. Support 4 FCE pins (2 dedicated pads + 2 additional FCE either dedicated pads if core limited or multiplexed on upper flash data bus if pad limited) | 1. 16 flash die support to be evaluated by packaging group for all products 2. 16 dies might require a bus switch for performance |
| Operating Power  (card level) | 1. 3.3v MS Duo/M2 Serial 65mA 2. 3.3v MS Duo/ M2 x4 100mA 3. 1.8v M2 serial/x4 100mA 4. 3.3V MS ProHG x4 100mA 5. 3.3V MS ProHG x8 200mA 6. eMS/eM2 x4 150mA 7. SD Normal Speed/High Speed 100mA/200mA 8. Lightning 200mA 9. SD UHS-50 400mA 10. SD UHS-104 800mA 11. eMMC (not side loading) Class0 12. eMMC (side loading) >=Class4 (as low as possible) | 1. Problematic to meet 65mA 2. Measurement method:   SD - max average over 16 mS window  MS - max average over 1 mS window  Currently in the SDA mechanical addenda 800mA is TBD for all form factors |
| Operating Power  (controller) | 1. Controller power to be defined to meet the product level power requirements based on the controller and flash activities within the 16ms measured window |  |
| Standby Power  (controller) | 1. MS Pro/M2(room T) 90uA 2. SD (typ) 50uA (80uA if capless regulator with <4nF internal capacitance) - desired 3. SD (across PVT) 750uA – desired 4. MS (across temp) 750uA | 1. MS card level 250uA single die (can go as high as 1mA) 2. SD card level (room temp) 350uA 3. SD controller standby to be finalized based on ASIC yield results |
| Analog Requirements | 1. On-chip *capless* core regulator designed to eliminate the need for an external regulator capacitors |  |
| Controller Memory Sizes | * SBRAM: 72KB (32KB SPR + 40KB BRAM) * MRAM: 128KB (Resident 108KB + ORAM 20KB) * ROM: 64KB |  |
| ECC | * 42bit/2K BCH ECC error correction * 52bit/2K BCH ECC error correction (32nm X2/X1) * 122bit/2K BCH ECC error correction (32nm X3, 24nm X2, possibly 24nm X3) |  |
| Endurance Requirement for eMMC 4.4 | 1. 100K P/E cycles for binary cache, 3K P/E cycles for other 2. DR (55C): 1 year for fresh device and 3 months after device wears out for binary cache, 10 years for fresh device and 1 year after device wears out for other. |  |
| Packaging | 1. SIP for uSD and M2 2. SD SIP 3. Duo SIP (ProHG SIP has the same dimensions but a different terminal definition) 4. 48 BGA production package (for SD SMT) 5. iNAND JEDEC BGA packages 6. 256BGA (engineering package) |  |
| Peripherals/ GPIO | 1. UART Tx (Rx not mandatory) 2. JTAG |  |
| Design for Manufacture | 1. Flash-tristate function | Needed for flash testing of multi-dies and for RMA/FA |
| Operating Conditions | 1. MS Pro -25C to 85C 2. SD -25C to 85C 3. eMMC -40C to 85C 4. MS HV 2.7V to 3.6V 5. MS LV 1.7V to 1.95V 6. SD HV 2.7V to 3.6V 7. eSD /eMMC Dual voltage 2.7V to 3.6V, 1.7V/1.65V(eMMC) to 1.95V |  |
| Storage Conditions | 1. eMMC -55°C to +125°C |  |
| Reliability | 1. SD/MS host pins 4kV HBM JEDEC 22a114d 2. SD/MS host pins 200V MM JEDEC 22a115a 3. SD/MS host pins 500V CDM in the final product form factor per JEDEC spec 22c101c 4. Embedded product pins 2kV HBM per JEDEC spec 22a114d 5. Embedded product pins 500V CDM per JEDEC spec 22c101c on either embedded product or engineering test package. Not test pads. 6. All non-host pins that will be wire bonded in any product configuration 1kV HEDEC HBM 7. All pads 200V CDM on the die that are probed or bonded during production test or manufacturing in the engineering test package. | See Appendix B |
| Compatibility | 1. Backward compatibility required at the card level. |  |
| MS Specific Requirements | 1. MagicGate MG-R |  |
| SDMMC Specific Requirements | 1. SDA Spec 3.0 Specification 2. eSD 2.1 Specification 3. eMMC 4.4 Specification 4. AFM support – AFM features and priority will be defined in details in the product ERD |  |
| SD Product Priority | * uSD/SD BL with 32nm X3 (ACT Apr/10) and eMMC 4.4 with 32nm X2 (ES Jan/10) * uSD Ultra with 32nm X3 dual die operation  1. All the rest of the listed SD products |  |
| MS Product Priority | 1. M2 and MS Duo BL with 32nm 32Gb X3 2. ProHG 30/30  * All the rest of the listed MS products |  |

# Section IV. Risks

|  |  |  |  |
| --- | --- | --- | --- |
| **Risk** | **Details** | **Level** | **Action** |
| BCH ECC | 122 BCH ECC is still not approved for 32nm X3 Memory | High |  |
| UHS and MMC4.4 | IO development and analog for SD UHS50 and MMC 4.4 | Med |  |
| BE FW Development | * New Gen6 development * Gen6 with 32nm X3 memory * Gen6 over PhoenixC2 architecture * MMC4.4 support | High |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

# Section V. Development Cost

**Engineering Resource requirements**

* Packaging Resources:

1Q09 – 1 man-month - SDUS

2Q09 – 3 man.months – SUDS + SDTW + SDSS

3Q09 - 3 man.months – SUDS + SDTW + SDSS

4Q09 – 2 man.months

1Q10 – 1 man.month



# Section VI. Appendix – Major Decisions

1. ROI justification for adding MS-HG:  
   Added cost 0.2 cents.  
   200M total P2 cards.  
   1.3M combined MS ProHG, MS VideoHD, MS Ultra cards that need to use either P2 or ComboS4E.  
   P2 cost: 11 cents.  
   ComboS4E cost: 41 cents.  
   Added cost of 200M cards total = 0.2 cents \* 200M = 400K$.  
   Realized savings from using P2 instead of ComboS4E on 1.3M MS cards = 30 cents \* 1.3M = 390K$  
     
   🡺 Breakeven in terms of cost. No added risk and schedule impact to P2 ASIC development.

# Section VII. Appendix – Open Issues

# Appendix A MMC random performance

* 52Mhz, 8-bit interface
* Write: 50 accesses per second. Should be verified on 512B/1K/2K/4K/8K chunk sizes.
* Read: 1000 accesses per second. Should be verified on 512B/1K/2K/4K/8K chunk sizes.
* Random sector address. Address can be unaligned to chunk size.
* Across all media
* Nokia use case: repeat the test 10K times, one chunk size per test (chunk sizes not interleaved):

Numebr of accesses = 10000

Chunk\_size = 512Bytes

While (chunk\_size < 16Kbytes)

{

            For (i=0;i< Numebr of accesses;i++)

{

            Sector Address = (Random(seed)) % (device total capacity in sectors)

            //Start measure time

            Write(Sector address, chunk size) OR Read(Sector address, chunk size)

            //stop measure time

            i++

}

Calculate Min, Max and average time for the current chunk\_size.

Calculate Min, Max, average IOS per second (based on total data that was read / written (chunk\_size \*  number of accesses) and performance measured)

Chunk\_size = chunk\_size\*2

}

# Appendix B ESD Requirements



# Appendix C Memory Configurations

|  |
| --- |
| FV\_32nm\_32G\_ABL\_D3\_1D |
| FV\_32nm\_32G\_ABL\_D3\_2D |
| FV\_32nm\_32G\_ABL\_D3\_4D |
| FV\_32nm\_32G\_ABL\_D3\_8D |

FV\_32nm\_32G\_ABL\_D3\_16D

|  |
| --- |
| FV\_32nm\_32G\_ABL\_ED3\_1D |
| FV\_32nm\_32G\_ABL\_ED3\_2D |
| FV\_32nm\_32G\_ABL\_ED3\_4D |
| FV\_32nm\_32G\_ABL\_ED3\_8D |

FV\_32nm\_32G\_ABL\_ED3\_16D

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  | | --- | | FV\_32nm\_16G\_ABL\_D2\_1D | | FV\_32nm\_16G\_ABL\_D2\_2D | | FV\_32nm\_16G\_ABL\_D2\_4D | | FV\_32nm\_16G\_ABL\_D2\_8D |   FV\_32nm\_16G\_ABL\_D2\_16D   |  | | --- | | FV\_32nm\_32G\_ABL\_D2\_1D | | FV\_32nm\_32G\_ABL\_D2\_2D | | FV\_32nm\_32G\_ABL\_D2\_4D | | FV\_32nm\_32G\_ABL\_D2\_8D |   FV\_32nm\_32G\_ABL\_D2\_16D  FV\_32nm\_64G\_ABL\_ED3\_1D |
| FV\_32nm\_64G\_ABL\_ED3\_2D |
| FV\_32nm\_64G\_ABL\_ED3\_4D |
| FV\_32nm\_64G\_ABL\_ED3\_8D |

FV\_32nm\_64G\_ABL\_ED3\_16D

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  | | --- | | FV\_32nm\_16G\_ABL\_D1\_1D | | FV\_32nm\_16G\_ABL\_D1\_2D | | FV\_32nm\_16G\_ABL\_D1\_4D | | FV\_32nm\_16G\_ABL\_D1\_8D |   FV\_32nm\_16G\_ABL\_D1\_16D   |  |  |  |  |  | | --- | --- | --- | --- | --- | | |  | | --- | | FV\_24nm\_64G\_ABL\_D2\_1D | | FV\_24nm\_64G\_ABL\_D2\_2D | | FV\_24nm\_64G\_ABL\_D2\_4D | | FV\_24nm\_64G\_ABL\_D2\_8D |   FV\_24nm\_64G\_ABL\_D2\_16D | | |  | | --- | | FV\_24nm\_32G\_ABL\_D2\_1D | | FV\_24nm\_32G\_ABL\_D2\_2D | | FV\_24nm\_32G\_ABL\_D2\_4D | | FV\_24nm\_32G\_ABL\_D2\_8D |   FV\_24nm\_32G\_ABL\_D2\_16D |   **ASIC Only (including ROM):** |
| Samsung\_42nm\_16G\_D2\_1D |

Samsung\_42nm\_16G\_D2\_2D

|  |
| --- |
| FV\_43nm\_16G\_ABL\_D2\_1D |
| FV\_43nm\_16G\_ABL\_D2\_2D |
| FV\_43nm\_16G\_ABL\_D2\_4D |
| FV\_43nm\_16G\_ABL\_D2\_8D |

FV\_43nm\_16G\_ABL\_D2\_16D

|  |
| --- |
| FV\_43nm\_32G\_ABL\_D2\_1D |
| FV\_43nm\_32G\_ABL\_D2\_2D |
| FV\_43nm\_32G\_ABL\_D2\_4D |
| FV\_43nm\_32G\_ABL\_D2\_8D |

FV\_43nm\_32G\_ABL\_D2\_16D

|  |
| --- |
| FV\_43nm\_8G\_ABL\_D2\_1D |
| FV\_43nm\_8G\_ABL\_D2\_2D |
| FV\_43nm\_8G\_ABL\_D2\_4D |
| FV\_43nm\_8G\_ABL\_D2\_8D |

FV\_43nm\_8G\_ABL\_D2\_16D

|  |
| --- |
| FV\_43nm\_16G\_ABL\_D1\_1D |
| FV\_43nm\_16G\_ABL\_D1\_2D |
| FV\_43nm\_16G\_ABL\_D1\_4D |
| FV\_43nm\_16G\_ABL\_D1\_8D |

FV\_43nm\_16G\_ABL\_D1\_16D

24nm X3 dies – up to 16 dies (as possible)

Samsung 3xnm X2/X3 – ASIC support, including ROM, for all available datasheets up to date (those that toggle mode is not mandatory)

# Appendix D UHS-104 support limitations and constraints

TBD – waiting for ASIC inputs